3rd SEM
(Paper-VII)

LESSON PLAN

3rd sem Sub: phy(hons) No. of Periods / Weeks :

Month	Paper/ Unit	Topics assigned	Page N
2	3	4	5
Feb	P-VII Unit-II	Bipolar Junction transistors • NPN - Transistor, NPN Transistor common Base transformer Load line Analysis of transistor, D.C load, Amplifiers - feedback amplifiers stabilisation, fixed Bias, Transistor as 2 port Network, classification A, B & C Amplifiers	

Signature of Teacher

PROGRESS

Sl. No.	Date	Time	Topics covered (If class not taken, mantion the reasons)	Signature of Teacher
1	2	3	4	5
	3.2.21	10-11	Introduction for self study	
	5.2.21	-do-	Discussed and Revision about • NPN, PNP - Transistor, connections Transferm, D-C load.	
	7.2.21	-do-	Discuss & Revisions (*) Amplifiers - transfer amplifiers classification, types of class A, B & C Amplifiers	
	8.2.21	-do-	Revision	
	9.2.21	-do-	Doubt clear with some question	

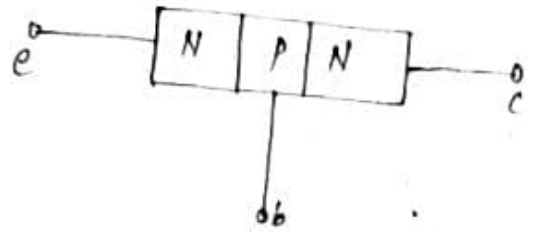
N.B. At the end of every week, It is be countersigned by HOD and the end of every month, It is to

CHAP-3 BIPOLAR JUNCTION TRANSISTORS

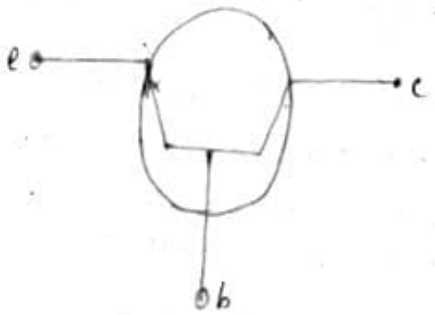
NPN-TRANSISTOR

An NPN-transistor consists of two PN-Junctions formed by sandwiching a P-type semiconductor between two N-type semiconductors.

The diagram for an NPN-transistor is shown below.



The symbolic diagram of an NPN-transistor is shown below.

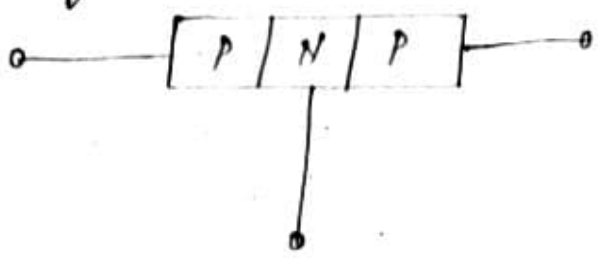


The emitter is shown by an arrow which represents the direction of emitter current when the emitter is forward biased. In an NPN-transistor the current flows out of the emitter.

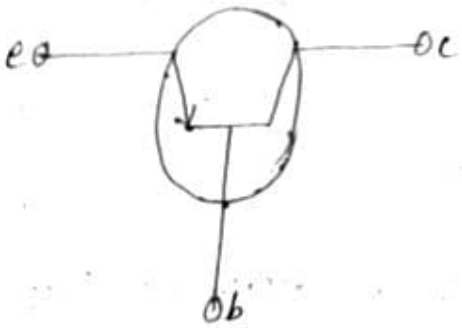
PNP-TRANSISTOR

A PNP-transistor consists of two PN-Junctions formed by sandwiching an N-type semiconductor b/w two P-type semiconductors.

The diagram of a PNP-transistor is shown below.

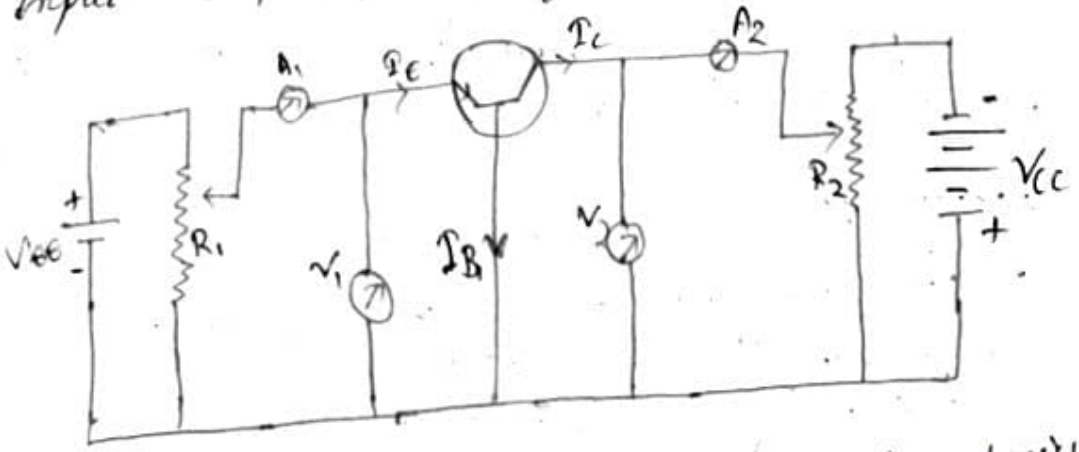


The symbolic diagram of a PNP-transistor is shown below.



characteristics of common Base configuration

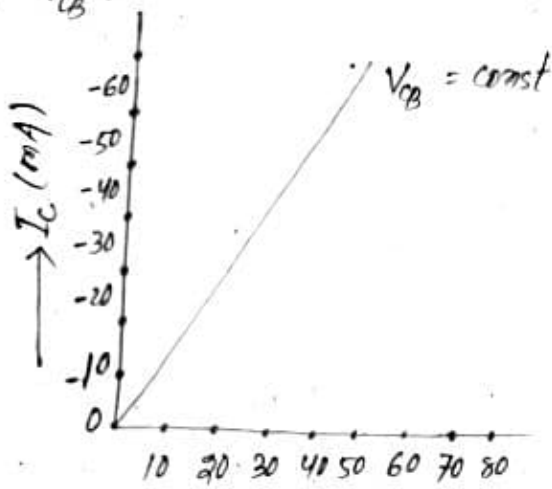
The important characteristics of common base configuration are input characteristics, output characteristics and transfer characteristics. The circuit diagram to study the characteristics of a PNP-transistor in common base configuration is shown in the fig-3.15. Voltmeters and ammeters are used to measure the input and output voltages and currents.



(Circuit diagram to study CB characteristics)

Common Base Transfer characteristics

The transfer characteristics for common base configuration is the curve between collector current I_C and emitter current I_E at constant collector base voltage V_{CB}.

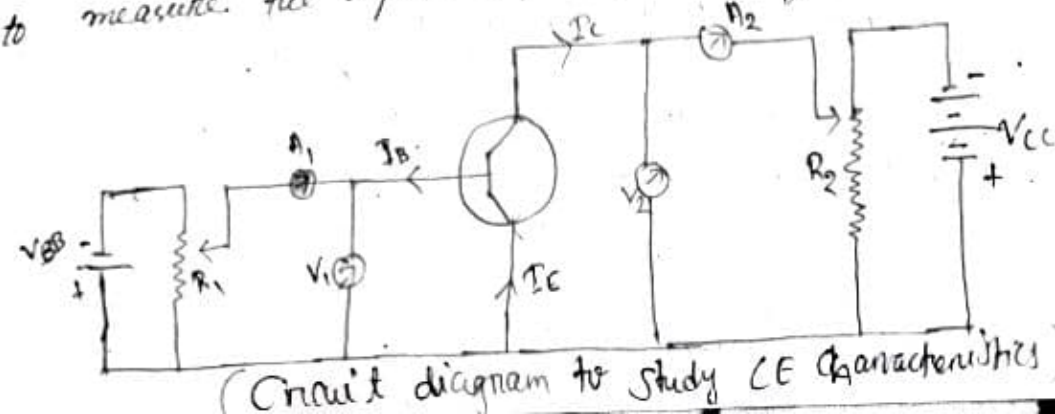


[fig: 3.18]

The transfer characteristics for common base configuration is shown in the fig. 3.18. It is a straight line. It is very useful in determining the effect of change in emitter current in the output.

characteristics of common Emitter configuration

The important characteristics of common emitter configuration are input characteristics, output characteristics and transfer characteristics. The circuit diagram to study the characteristics of a PNP-transistor in common emitter configuration is shown in the figure - 3.19. voltmeters and ammeters are used to measure the input and output voltages and currents



(Circuit diagram to study CE characteristics

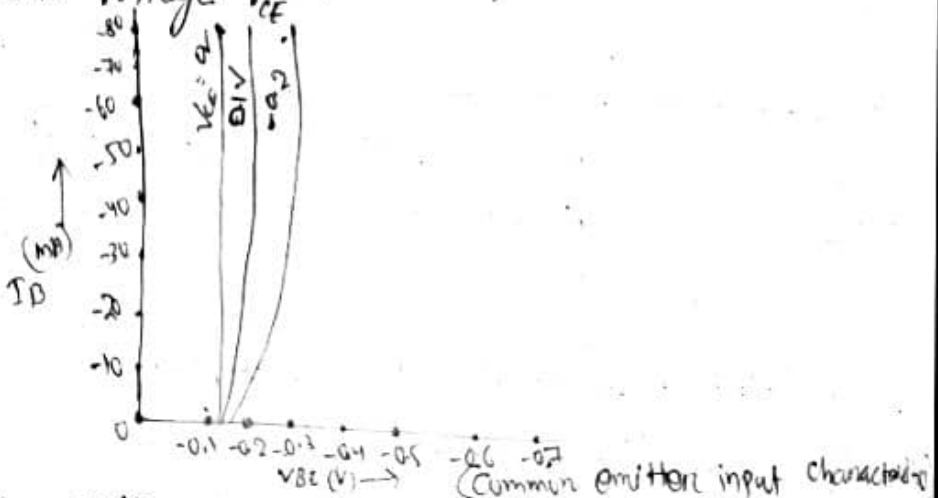
The input characteristics for common emitter configuration is the curve between base current I_B and base-emitter voltage V_{BE} at constant collector-emitter voltage V_{CE}.

The common emitter input characteristics for $V_{CE} = 0V$, $-0.1V$ and $-0.2V$ are shown in the fig. 3.20. The following points may be noted from the common-emitter input characteristics.

(i) The base current I_B increases rapidly with the increase in base emitter voltage V_{BE}.

(ii) The common emitter, input characteristics are similar to that of a forward biased junction diode.

(iii) The base current is almost independent of collector-emitter voltage V_{CE}.



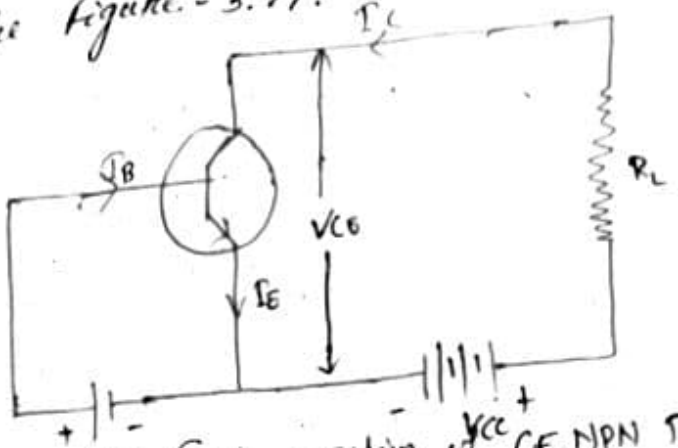
Common emitter input characteristics

LOAD LINE ANALYSIS OF TRANSISTOR

It is generally necessary to find out the collector current for different collector-emitter voltages in the transistor circuit circuit analysis. The load line method is a convenient method of determine the collector current at any desired collector-emitter voltage from the common emitter output characteristics. The load line method is an easier method and is frequently used in the analysis of transistor circuit applications.

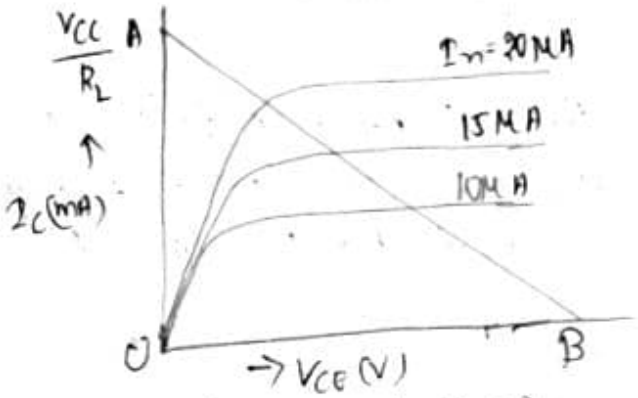
D.C. Load line

. consider a common-emitter NPN-transistor circuit with no input signal applied. Hence. D.C. condition prevails in the input and output circuits of the transistor. The D.C. operation of a common-emitter NPN-transistor is shown in the figure-3.27.



(DC operation of CE NPN transistor)

The common emitter output characteristics of the NPN-transistor with no input signal for $I_B = 10\mu A$, $15\mu A$ and $20\mu A$ are shown in the figure-3.28.



(D.C Load line)

The value of collector-emitter voltage at any instant is given by,

$$V_{CE} = V_{cc} - I_c R_L \quad \text{---- (1)}$$

This is a first degree equation and it can be represented by a straight line on the output characteristics. This straight line is known as D.C. load line. The slope of the D.C. Load line is $-R_L$ and intercept along V_{CE} axis is V_{cc}.

The two end points of the D.C. load line can be located as:

(i) If the collector current $I_c = 0$ then the collector-emitter voltage is maximum.

using eqn (1) we get,

$$V_{CE} = V_{cc} = \text{maximum} \quad ---- (2)$$

This gives the end point B on the V_{CE} axis as depicted in fig 3.28.

(ii) If the collector-emitter voltage $V_{CE} = 0$ then the collector current is maximum.

using eqn (1) we get,

$$0 = V_{cc} - I_c R_L$$

$$\text{or} \quad V_{cc} = I_c R_L$$

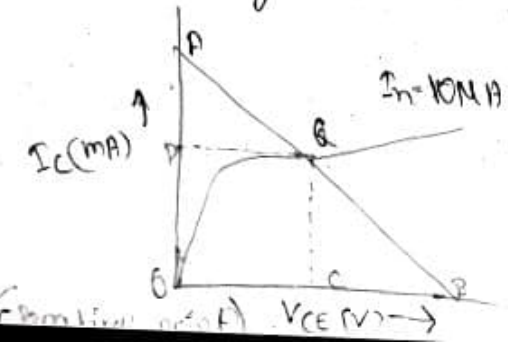
$$\text{or} \quad I_c = \frac{V_{cc}}{R_L} = \text{maximum} \quad ---- (3)$$

This gives the end point A on the I_c axis as depicted in fig-3.28. The points A and B are joined to construct the D.C. load line.

Q-point

Q point is defined as the zero signal valu of the collector current I_c and the collector-emi voltage. V_{CE}.

In the absence of signal the output charact of common-emitter NPN-transistor for $I_B = 10\mu$ is shown in the figure - 3.29.



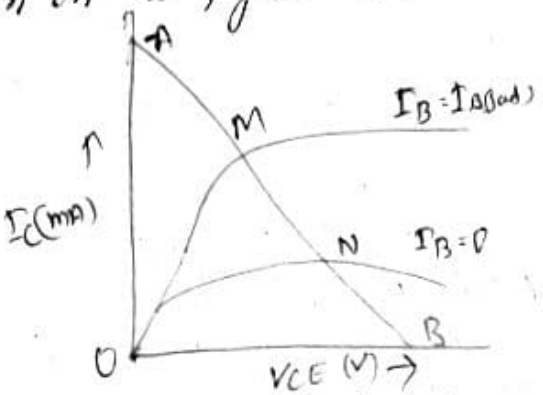
Q-point is the point at which the D.C. load line intersects with the output characteristics. It is denoted by the point Q. Q-point is known as quiscent (silent) point because it is a point on the output characteristics when there the transistor is silent ie, in the absence of the signal. Q-point is also known as operating point because when the input signal is applied, the variations of I_C and V_{CE} take place about Q-point.

For $I_B = 10\,\mu A$ the zero signal values are

$V_{CE} = 0$ volt, $I_C = 0$ mA.

ACTIVE, CUT-OFF AND SATURATION REGIONS

The common emitter output characteristics of an NPN-transistor along with the D.C. load line are shown in the figure - 3.30.



Saturation point

Saturation point is the point at which the D.C. load line intersects the $I_B = I_{B(sat)}$ curve. The based current is maximum at saturation point and hence the collector current is also maximum. This point is denoted by the point M. At saturation point the collector-base junction is no longer remains reserve biased and hence the normal action of transistor is lost and I_C axis is known as saturation region.

At saturation point M

$V_{CE} = V_{CE(sat)} = V_{knee}$

$I_{C(sat)} \simeq \frac{V_{CC}}{R_L}$

Cut-off point

cut-off point is the point at which the D.C. load line intersects the $I_B = 0$ curve. At this point only small collector current exists and the base-emitter junction no longer remains forward biased. Hence normal transistor action is lost. It is denoted by the point N. The region below the $I_B = 0$ curve is known as cut-off region.

At saturation point N

$V_{CE(sat)} \simeq V_{CC}$

Active Region

Active region is the region between saturation region and cut-off region. In the active region the emitter-base junction is forward biased and the collector base junction is reverse biased and the transistor works normally. Hence the transistor can remain in three states namely saturated, cut-off and active states. The state of a transistor is determined by the states of emitter-base junction and collector-base junction).

If the transistor is in saturated state, the emitter-base junction and collector-base junction are in ON states.

If the transistors is in cut-off state, the emitter-base junction and collector-base junction are in off states.

If the transistor is in active state, then the emitter-base junction is in ON state and the collector-base junction is in OFF state.

AMPLIFIERS (chap-4)

Faithful Amplication

faithful amplification is the process of increasing the strength of a weak signal without any change in its shape.

In order to achieve faithful amplification the transistor amplifier must satisfy the following three basic conditions.

(i) Proper zero signal collector current

(ii) Proper minimum base - emitter voltage at any instant.

(iii) Proper minimum collector - emitter voltage at any instant.

Transistor Biasing

It is the proper flow of zero signal collector current and the maintenance of proper collector-emitter voltage during the passage of signal.

The basic purpose of transistor biasing is the proper functioning of the transistor. The transistor functions properly if the emitter-base junction is properly forward biased and the collector-base junction is properly reverse biased during the all parts of the signal. This can be achived with a bias battery or associating a

circuit with a transistor. The circuit that provides transistor biasing is known as bias circuit.

STABILISATION

The collector current in a transistor varies quickly if the temp. varies and the transistor is replaced by another transistor of the same type.

Stabilisation is the process of making the operation point independent of temperature changes or variations in transistor parameters.

If stabilisation is done then the operating point (value of I_c and V_{ce}) is independent of variation in temp. or replacement of transistor.

The stabilization of operating point is ensured by a good biasing circuit. The stabilization of the operating point is required because of the following reason:

(i) Temperature variation

(ii) Variation in transistor parameters

(iii) Thermal runaway

(i) Temperature Variation

The collector current for common emitter transistor circuit is given by

$$I_c = \beta I_B + I_{CEO}$$

Now $$I_{CEO} = \frac{I_{CBO}}{1-\alpha}$$

$$\therefore I_c = \beta I_B + \frac{I_{CBO}}{1-\alpha}$$

Now $\frac{1}{1-\alpha} = (1+\beta)$

$\therefore I_c = \beta I_B + (1+\beta) I_{CBO}$.

The collector leakage current I_{CBO} is affected by the temp. variation. For germanium transistor the collector leakage current I_{CBO} is doubled when the temp. is increased through 10°C. Hence it is necessary to stabilize the operating point to hold the collector current I_c const. inspite of variation in temperature.

(ii) Variation in transistor parameters

The transistor parameters such as β and V_{BE} are not exactly the same for any two transistors is of the same type. Further V_{BE} decreases when temp. increases. If a transistors is replaced by another transistors of same type the operating point is changed due to the variations in β and V_{BE}. Hence it is necessary to stabilize the operating point to hold I_c const. inspite of variations in transistor parameters.

(iii) Thermal runway

The collector current for common emitter transistor connection is given by

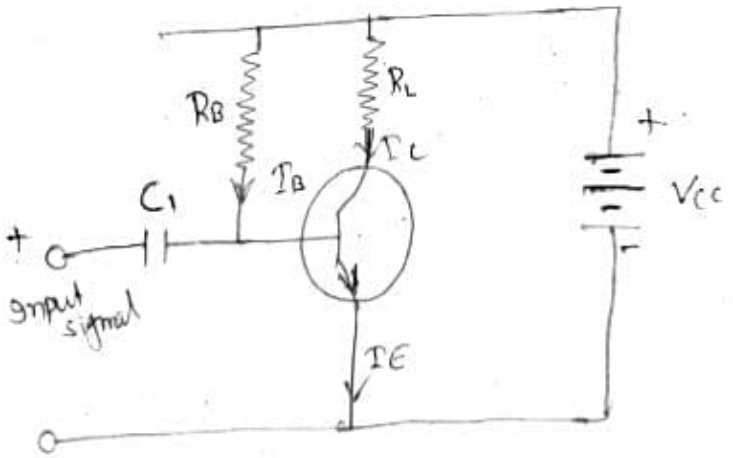
$$I_c = \beta I_B + (1+\beta) I_{CBO}$$

The flow of collector current causes production of heat inside the transistor. If stabilisation is not done then the collector leakage current I_{CBO} is increased then the collector current I_c is increased by $(1+\beta) I_{CBO}$. The increase in I_c will increase then the temp. of the transistor which will also cause increase in I_{CBO}.

Hence it is necessary to stabilize the operating point to hold I_c constant in order to avoid thermal runaway. This is done by causing the base current I_B to decrease with the increase in temp. by the modification of the circuit. It is clear that the decrease in βI_B will compensate for the increase in $(1+\beta) I_{CO}$ to get constant I_c. This is required in designing a biasing circuit.

FIXED BIAS

The fixed bias method is also known as base bias method. The circuit diagram for fixed bias method is given below. In fixed bias method a high resistance R_B is connected between the base and the positive terminal of the DC source of supply for NPN transistor in common emitter configuration. The single source of voltage V_{cc} makes the emitter-base junction forward biased and collector-base junction reverse biased.



(Fixed bias for CE configuration)

The voltage source V_{cc} also provides the zero signal base current and collector current. According to Kirchhoff's voltage law

$$V_{cc} = I_B R_B + V_{BE}$$

Where V_{BE} is the base-emitter voltage

$$\Rightarrow V_{cc} - V_{BE} = I_B R_B$$

$$\Rightarrow R_B = \frac{V_{cc} - V_{BE}}{I_B} \quad \text{——— (i)}$$

Since $V_{cc} >> V_{BE}$

$$\Rightarrow V_{cc} - V_{BE} \simeq V_{cc}$$

Using eqn (i) we get

$$R_B = \frac{V_{cc}}{I_B} \quad \text{——— (ii)}$$

$$\Rightarrow I_B = \frac{V_{cc}}{R_B}$$

∴ The base current is fixed by V_{cc} and R_B and for this cause this method is known as fixed bias method.

The collector current is given by

$$I_C = \beta I_B + (1+\beta) I_{CBO} \quad \text{——— (iii)}$$

Differentiating both sides with respect to the collector current we get,

$$1 = \beta \frac{dI_B}{dI_C} + (1+\beta) \frac{dI_{CBO}}{dI_C} \quad \text{——— (iv)}$$

Now $\frac{dI_C}{dI_{CBO}} = S$

where S is the stability factor.

$$\therefore \frac{dI_{CBO}}{dI_C} = \frac{1}{S}$$

Using eqn (iv) we get,

$$1 = \beta \frac{dI_B}{dI_C} + \frac{1+\beta}{S}$$

$$\Rightarrow 1 - \beta \frac{dI_B}{dI_C} = \frac{1+\beta}{S}$$

$$\Rightarrow S = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)} \quad \text{——— (v)}$$

In fixed bias method of biasing the transistor, the base current I_B is independent of the collector current I_C.

$$\therefore \frac{dI_B}{dI_C} = 0$$

Using eqn (v) we get,

$$S = 1+\beta \quad \text{——— (vi)}$$

$$\Rightarrow \frac{dI_C}{dI_{CBO}} + (1+\beta)$$

$$\Rightarrow dI_C = (1+\beta)\, dI_{CBO}$$

$\Rightarrow I_C$ changes $(1+\beta)$ times faster than I_{CBO}.

Advantages:-

The fixed bias method of biasing has the following advantages.

(i) Fixed bias circuit is very simple because only one high resistance is necessary.

(ii) The calculations are very simple to set the biasing condition.

(iii) There is no loading of the source by the biasing circuit because no resistor is used in base-emitter circuit.

Disadvantages :-

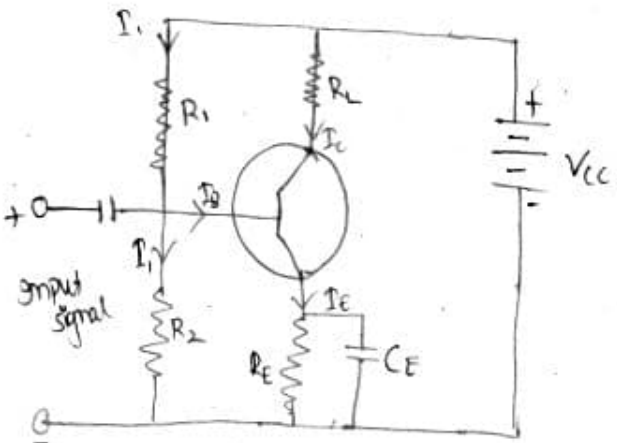
The fixed bias method of biasing has the following disadvantages.

(i) It provides poor stabilization because there is no means to stop the increase in Collector current due to increase in temperature and variation in transistor parameters.

(ii) It has poor thermal stability due to the large value of stability factor.

Voltage Divider Bias :-

The voltage divider bias is also known as self bias or emitter bias. The circuit diagram for voltage divider bias method of transistor ~~bias~~ biasing for Common-emitter Configuration is show in the figure-4.8 In this method of transistor biasing two resistances R_1 & and R_2 are connected across the supply voltage V_{cc} to provide biasing.



(Voltage divider bias for CE Configuration)

The supply voltage V_{cc} makes the base emitter junction forward biased and the base-collector junction reverse biased through the resistances R_1, R_2, R_E and R_L. The emitter resistance R_E provides stabilization.

The circuit is known as voltage divider bias circuit because the potential divider formed by resistances R_1 & R_2 biased the transistor. The voltage across the resistance R_2 makes the base emitter junction forward biased. This causes the zero signal base current I_B and hence the zero signal collector current I_C to flow.

If I_1 is the current flowing through R_1 then the current flowing through R_2 is also I_1 since the base current I_B is very small.

$$\therefore V_{CC} = I_1 (R_1 + R_2)$$

$$\Rightarrow I_1 = \frac{V_{CC}}{R_1 + R_2} \quad \text{——(i)}$$

Voltage across R_2 is given by

$$V_2 = I_1 R_2$$

$$\Rightarrow V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2 \quad \text{——(ii)}$$

According to Kirchhoff's voltage law

$$V_2 = V_{BE} + V_E$$

where V_{BE} is the base-emitter voltage and V_E is the voltage across R_E.

$$\therefore V_2 = V_{BE} + I_E R_E$$

$$\because V_E = I_E R_E$$

$$\Rightarrow V_2 - V_{BE} = I_E R_E$$

$$\Rightarrow I_E = \frac{V_2 - V_{BE}}{R_E} \quad \text{——(iii)}$$

Now $I_E = I_B + I_C$

$$\Rightarrow I_E \simeq I_C \quad \because I_B \text{ is very small}$$

Using equation (iii) we get

$$I_C = \frac{V_2 - V_{BE}}{R_E} \quad \text{——(iv)}$$

∴ I_C is independent of β and dependent on V_{BE}. In practice $V_2 >> V_{BE}$ and hence I_C is independent of V_{BE}. Thus I_C is almost independent of the transistor parameters. Therefore good stabilisation is ensured in this method.

Applying Kirchhoff's voltage law to the collector circuit

$$V_{CC} = I_C R_L + V_{CE} + I_E R_E$$

$$\Rightarrow V_{CC} = I_C R_L + V_{CE} + I_C R_E \quad \because I_E \simeq I_C$$

$$\Rightarrow V_{CC} = I_C (R_L + R_E) + V_{CE}$$

$$\Rightarrow V_{CE} = V_{CC} - I_C (R_L + R_E) \quad \text{---- (v)}$$

Using equation (iv) we get

$$V_2 - V_{BE} = I_C R_E$$

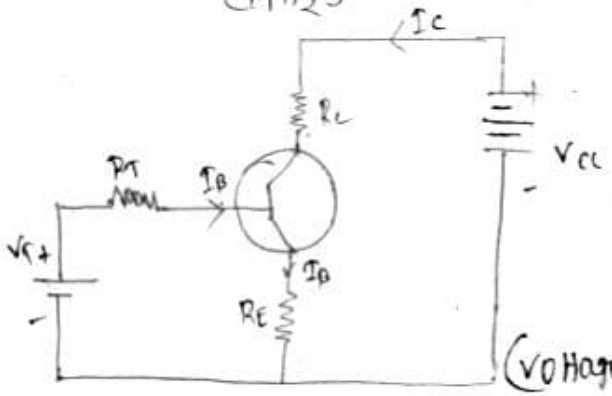
$$\Rightarrow V_2 = V_{BE} + I_C R_E \quad \text{---- (vi)}$$

If I_C increases due to increase in temp then the voltage across R_E increases since V_2 is independent of I_C, the value of V_{BE} decreases. Thus I_B decreases. The decrease in I_B tends to restore the original value of I_C. Hence excellent stabilisation is provided by the emitter resistance R_E in voltage divider bias circuit.

The DC. circuit to the left of the base terminal of the voltage divider bias circuit can be replaced by Thevenin's equivalent circuit as

Thevenin's equivalent voltage is given by

$$V_T = \left[\frac{V_{CC}}{R_1 + R_2}\right] R_2 \quad \text{---- (vii)}$$



(voltage divider bias circuit)

Thevenins equivalent resistance is given by

$$R_T = \frac{R_1 R_2}{R_1 + R_2} \quad \text{——— (viii)}$$

Applying kirchoff's voltage law to the base circuit

$$V_T = I_B R_T + V_{BE} + I_E R_E$$

$$\Rightarrow V_T = I_B R_T + V_{BE} + (I_B + I_C) R_E \quad \text{——— (ix)}$$

Differentiating both sides with respect to I_C we get

$$0 = R_T \frac{dI_B}{dI_C} + 0 + R_E \frac{dI_B}{dI_C} + R_E$$

$\because V_T$ = Constant, V_{BE} = Constant.

$$\frac{dV_T}{dI_C} = 0 \quad \& \quad \frac{dV_{BE}}{dI_C} = 0$$

$$\Rightarrow 0 = \frac{dI_B}{dI_C}(R_T + R_E) + R_E$$

$$\Rightarrow \frac{dI_B}{dI_C}(R_T + R_E) = -R_E$$

$$\Rightarrow \frac{dI_B}{dI_C} = -\frac{R_E}{R_T + R_E} \quad \text{——— (x)}$$

The stability factor for common-emitter configuration is given by

$$S = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)} \quad \text{——— (xi)}$$

Putting the value of $\left(\frac{dI_B}{dI_C}\right)$ from eqn (x) in eqn (xi) we get

$$S = \frac{1+\beta}{1-\beta\left(\frac{-R_E}{R_T + R_E}\right)}$$

$$\Rightarrow S = \frac{1+\beta}{1+\left(\frac{\beta R_E}{R_T + R_E}\right)}$$

$$\Rightarrow S = 1+\beta \Big/ R_T + R_E + \beta R_E \Big/ R_T + R_E$$

$$\therefore S = \frac{(1+\beta)(R_T + R_E)}{R_T + (1+\beta) R_E}$$

$$\therefore S = \frac{(1+\beta)\left(1 + \frac{R_T}{R_E}\right)}{(1+\beta) + \frac{R_T}{R_E}} \quad \text{---(xii)}$$

If $\frac{R_T}{R_E}$ is made very small then

$$1+\beta + \frac{R_T}{R_E} \simeq 1+\beta$$

and $1 + \frac{R_T}{R_E} \simeq 1$

Using equation (xii) we get

$$S = \frac{1+\beta}{1+\beta}$$

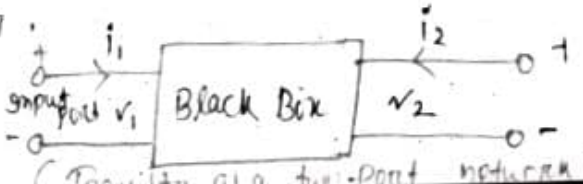
$$\therefore S = 1$$

This is the ideal value of S and it leads to maximum thermal stability.

The value of $\frac{R_T}{E_E}$ can be made very small by increasing the value of R_E and decreasing the value of R_T. The value of R_T can be decreased by decreasing the value of R_2. If the value of R_2 is small then the current drawn from V_{cc} is large. Hence there is a restriction on the choice of R_T.

Transistor As 2-Port Network :-

In transistor amplifier the alternating currents or voltages ie signals are applied to a pair of input terminals known as input terminal known as input port. The amplified signal is obtained from a pair of output terminals known as out put port of the transistor amplifier.

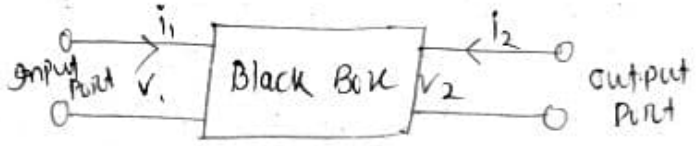


(Transistor as a two-Port network)

For a small amplitude of the input signal the working of the transistor is restricted to the linear region of output characteristic curve of the transistor. This linear working of the transistor amplifier can be studied analytically by regarding the transistor as a black box having a pair of input terminals and a pair of output terminals in any of the three modes. The terminal behaviour of transistor is determined by four variables and these variables are two signal voltages v_1 & v_2. The currents are taken as positive when they enter the transistor and taken as negative when they leave the transistor. The voltages are taken as positive from upper to lower terminals and taken as negative from lower to upper terminals.

Equivalent Circuit with Hybrid (H) Parameters :

Every linear circuit having an input port and an output port can be represented by a black box, as



(Linear circuit of transistor)

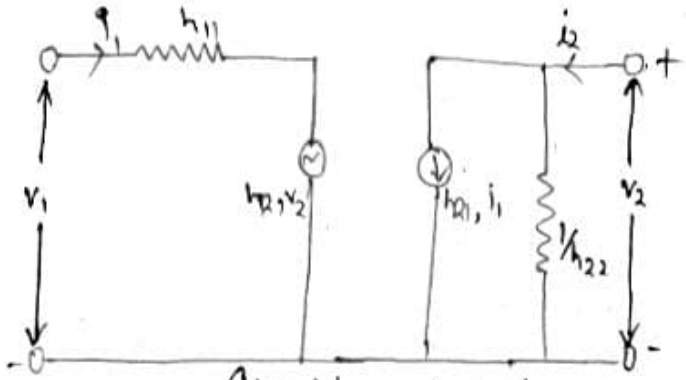
For a small signal amplifier the transistor circuit is a linear circuit. The circuit can be analysed by four variables. The four variables are input current i_1, output current i_2, input voltage v_1 and output voltage v_2. The current are assumed positive if they flow into the black box and -ve if they flow out of the black box. The voltages are assumed positive from the upper to the lower terminals and negative from the lower to the upper terminals. These are standard sign conventions

The input current i_1, and the output voltage v_2 are considered as the independent variables but the input voltage v_1 and output current i_2 are considered as dependent variables. The dependent variables of a transistor are related to the independent variables by the following equation.

$$v_1 = h_{11} i_1 + h_{12} v_2 \quad \text{——— (i)}$$

$$i_2 = h_{21} i_1 + h_{22} v_2 \quad \text{——— (ii)}$$

In these equations the constant h_{11}, h_{12}, h_{21} & h_{22} are known as hybrid parameters. The parameter h_{11} has the dimension of impedance and it is measured in ohm. The parameter h_{22}, has the dimension of admittance and it is measured in mho. The parameters h_{12} and h_{21} are dimensionless and unitless. These parameters are known as hybrid parameters because they have mixed dimensions.



(Hybrid equivalent Circuit of a transistor)

The parameter h_{11}

If $v_2 = 0$ then using eqn (i) we get

$$v_1 = h_{11} i_1$$

$$\text{or } h_{11} = \frac{v_1}{i_1} \quad \text{——— (iii)}$$

The parameter h_{11} is the ratio of input A.C voltage to input A.C Current and it represents the input impedance with the output port short circuited.

It is denoted by h_{ie} for common emitter mode h_{ib} for common base mode and h_{ic} for common collector mode.

It is measured in ohm.

The parameter h_{12}

If $i_1 = 0$ then using eqn(i) we get

$$v_1 = h_{12} v_2$$

$$\Rightarrow h_{12} = \frac{v_1}{v_2} \quad \text{---(iv)}$$

The parameter h_{12} is the ratio of input A.C voltage to output A.C voltage and it represents reverse voltage transfer ratio with input port open. It is denoted by h_{re} for common emitter mode, h_{rb} for common base mode and h_{rc} for common collector mode.

It is unitless.

The parameter h_{21}

If $v_2 = 0$ then using eqn(ii) we get

$$i_2 = h_{21} i_1$$

$$\Rightarrow h_{21} = \frac{i_2}{i_1} \quad \text{---(v)}$$

The parameter h_{21} is the ratio of output A.C current to input A.C. current and it represents forward current transfer ratio with output port short circuited. It is denoted by h_{fe} for common emitter mode, h_{fb} for common base mode & h_{fc} for common collector mode.

It is unitless.

The parameter h_{22}:

If $i_1 = 0$ then using eqn (ii) we get

$$i_2 = h_{22} v_2$$

$$\Rightarrow h_{22} = \frac{i_2}{v_2} \quad \text{---(vi)}$$

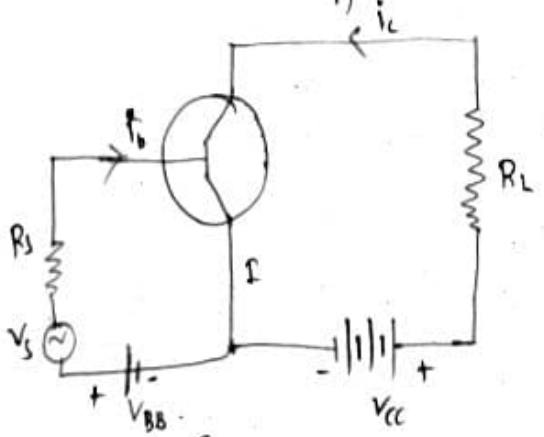
The parameter h_{22} is the ratio of output A.C curr

to output AC voltage and it represents output admittance with input port open. It is denoted by h_{oe} for common emitter mode, h_{ob} for common base mode and h_{oc} for common collector mode.

(It is measured in mho).

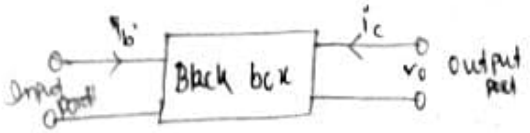
Hybrid Equivalent Circuit of Single Stage CE Amplifier:

The circuit diagram of a single stage common emitter amplifier using an NPN- transistor is,



(Single stage CE amplifier)

For the analysis of small signal voltage the single stage CE amplifier is a linear circuit and it can be represented by a black box.



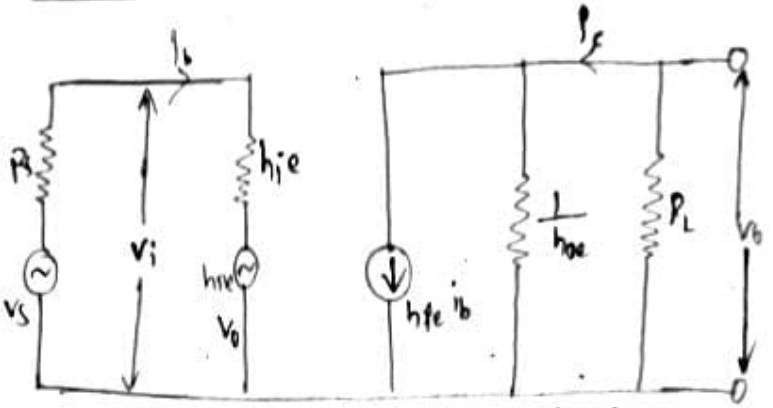
(Linear circuit)

The dependent variables of the transistor in CE configuration are related to the independent variables by the following relations.

$$v_i = h_{ie}\, i_b + h_{re}\, v_o \quad \text{---(i)}$$

$$i_c = h_{fe}\, i_b + h_{oe}\, v_o \quad \text{---(ii)}$$

They hybrid equivalent circuit of the single stage CE amplifier with signal source v_s, source resistance R_s and load resistance R_L is,



(Hybrid equivalent circuit of single stage CE amplifier)

Analysis of single stage CE amplifier using hybrid model.

Input impedance, output impedance, current gain, voltage gain and power gain of a single stage CE amplifier can be find out in terms of hybrid parameters.

Input Impedance :-

Input impedance is defined as the ratio of input voltage to input current.

It is given by

$$Z_{ie} = \frac{v_i}{i_b} \quad \text{——(iii)}$$

Putting the value of v_i from eq^n(i) we get

$$Z_{ie} = \frac{h_{ie} i_b + h_{re} v_o}{i_b} \quad \text{——(iv)}$$

Now $v_o = -i_c R_L$

Using eq^n(iv) we get

$$Z_{ie} = \frac{h_{ie} i_b - h_{re} i_c R_L}{i_b}$$

$$\Rightarrow Z_{ie} = h_{ie} - h_{re} R_L \left(\frac{i_c}{i_b}\right) \quad \text{——(v)}$$

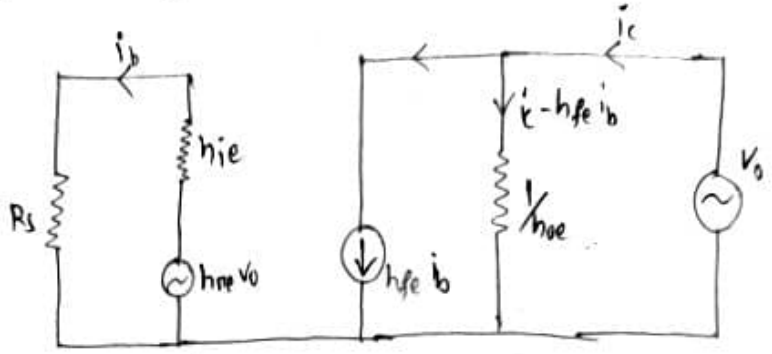
Now $\frac{i_c}{i_b} = A_{ie}$

Using eq^n(v) we get

$$Z_{ie} = h_{ie} - h_{re} R_L A_{ie} \quad \text{——(vi)}$$

Output impedance :-

In order to find out the output impendance the signal source V_s is removed and replaced by source resistance R_s and the load R_L is removed and replaced by A.C. voltage source V_0.



(Equivalent circuit to find output impedance.)

Output impedance is defined as the ratio of output voltage to output current.

It is given by

$$Z_{oe} = \frac{V_0}{i_c} \quad \text{——(vii)}$$

Applying kirchhoff's current law to the output circuit

$$i_c = h_{fe} i_b + h_{oe} V_0 \quad \text{——(viii)}$$

Applying Kirchhoff's voltage law to the input circuit

$$(R_s + h_{ie}) i_b + h_{re} V_0 = 0$$

$$\Rightarrow (R_s + h_{ie}) i_b = -h_{re} V_0$$

$$\Rightarrow i_b = -\frac{h_{re} V_0}{R_s + h_{ie}} \quad \text{——(ix)}$$

Putting the value of i_b in eqn (viii) we get

$$i_c = h_{oe} V_0 - \frac{h_{fe} h_{re} V_0}{R_s + h_{ie}}$$

$$\Rightarrow i_c = V_0 \left[h_{oe} - \frac{h_{fe} h_{re}}{R_s + h_{ie}} \right]$$

$$\Rightarrow \frac{i_c}{V_0} = h_{oe} - \frac{h_{fe} h_{re}}{R_s + h_{ie}} \quad \text{——(x)}$$

Now $\frac{i_c}{V_0} = \frac{1}{Z_{oe}}$

Using eqn (x) we get

$$\frac{1}{Z_{oe}} = h_{oe} - \frac{h_{fe}\, h_{re}}{R_s + h_{ie}}$$

$$\Rightarrow \frac{1}{Z_{oe}} = \frac{h_{oe}(R_s + h_{ie}) - h_{fe}\, h_{re}}{R_s + h_{ie}}$$

$$\Rightarrow Z_{oe} = \frac{R_s + h_{ie}}{h_{oe}(R_s + h_{ie}) - h_{fe}\, h_{re}}$$

$$\Rightarrow Z_{oe} = \frac{R_s + h_{ie}}{h_{ie}\, h_{oe} + h_{oe} R_s - h_{fe}\, h_{re}} \quad \text{——— (xi)}$$

Current gain :-

The current gain is defined as the ratio to output current to input current.

It is given by

$$A_{ie} = \frac{i_c}{i_b} \quad \text{——— (xii)}$$

The effective impedance of $\frac{1}{h_{oe}}$ and R_L is given by

$$\frac{1}{Z} = \frac{1}{\frac{1}{h_{oe}}} + \frac{1}{R_L}$$

$$\Rightarrow \frac{1}{Z} = h_{oe} + \frac{1}{R_L}$$

$$\Rightarrow \frac{1}{Z} = \frac{1 + h_{oe} R_L}{R_L}$$

$$\Rightarrow Z = \frac{R_L}{1 + h_{oe} R_L} \quad \text{——— (xiii)}$$

It is clear that

voltage across R_L = voltage across Z

$\Rightarrow i_c R_L = h_{fe} i_b Z$

Putting the value of z from eqn (xiii) we get

$$i_c \cdot R_L = h_{fe}\, i_b \left(\frac{R_L}{1+h_{oe} R_L}\right)$$

$$\Rightarrow \frac{i_c}{i_b} = \frac{h_{fe}}{1+h_{oe} R_L}$$

$$\Rightarrow A_{ie} = \frac{h_{fe}}{1+h_{oe} R_L} \quad \text{——— (xiv)}$$

Voltage Gain :-

The voltage gain is defined as the ratio of output voltage to input voltage.

It is given by.

$$A_{ve} = \frac{V_0}{V_i} \quad \text{——— (xv)}$$

Now $V_0 = -i_c R_L$

$$\therefore A_{ve} = \frac{-i_c R_L}{V_i}$$

$$\Rightarrow A_{ve} = -\left(\frac{i_c}{i_b}\right)\left(\frac{i_b}{V_i}\right) R_L$$

$$\Rightarrow A_{ve} = -A_{ie}\left(\frac{1}{z_{ie}}\right) R_L$$

$$\Rightarrow A_{ve} = -\frac{A_{ie} R_L}{z_{ie}} \quad \text{——— (xvi)}$$

Putting the values of A_{ie} & z_{ie} from eqn (xiv) & (vi) we get,

$$A_{ve} = -\frac{h_{fe} R_L}{1+h_{oe} R_L} \times \left(\frac{1}{h_{ie} - h_{re} R_L A_{ie}}\right)$$

Again putting the value of A_{ie} from (xiv) we get

$$\Rightarrow A_{ve} = -\frac{h_{fe} R_L}{(1+h_{oe} R_L)\left(h_{ie} - \frac{h_{re} R_L h_{fe}}{1+h_{oe} R_L}\right)}$$

$$\Rightarrow A_{ve} = -\frac{h_{fe} R_L}{h_{ie}(1+h_{oe} R_L) - h_{re} R_L h_{fe}}$$

$$\Rightarrow A_{ve} = -\frac{h_{fe} R_L}{h_{ie} + h_{ie} h_{oe} R_L - h_{re} R_L h_{fe}}$$

$$\Rightarrow A_{ve} = -\frac{h_{fe} R_L}{h_{ie} + (h_{ie} h_{oe} - h_{re} h_{fe}) R_L} \quad \text{——(xvii)}$$

Now $h_{ie} h_{oe} - h_{re} h_{fe} = \Delta h$ ——(xviii)

Using equation (xvii) we get

$$A_{ve} = -\frac{h_{fe} R_L}{h_{ie} + \Delta h R_L} \quad \text{——(xix)}$$

Power Gain :-

The power gain is defined as the ratio of output power to input power.

It is given by

$$A_{pe} = \frac{P_0}{P_i} \quad \text{——(xx)}$$

Input power is given by

$$P_i = V_i i_b$$

Output power is given by

$$P_0 = V_0 i_c$$

Using equation (xx) we get

$$A_{pe} = \frac{V_0 i_c}{V_i \cdot i_b}$$

$$\Rightarrow A_{pe} = \left(\frac{V_0}{V_i}\right)\left(\frac{i_c}{i_b}\right) \quad \text{——(xxi)}$$

$$\Rightarrow A_{pe} = A_{ve} A_{ie} \quad \text{——(xxi)}$$

Using equation (xvi) the magnitude of A_{ve} is given by

$$A_{ve} = \frac{A_{ie} R_L}{z_{ie}}$$

$$\therefore A_{pe} = \frac{A_{ie}^2 R_L}{z_{ie}} \quad \text{——(xxii)}$$

Putting the value of A_{ve} and A_{ie} from (xix) & (xiv) in (xxii), we get

$$A_{fe} = \left(\frac{h_{fe} R_L}{h_{ie} + \Delta h R_L}\right)\left(\frac{h_{fe}}{1 + h_{oe} R_L}\right)$$

$$\Rightarrow A_{fe} = \frac{h_{fe}^2 R_L}{(1 + h_{oe} R_L)(h_{ie} + \Delta h R_L)} \quad \text{---------- (xiii)}$$

Classification of Class A, B & C Amplifiers :-

Class A Amplifiers

Class A amplifiers is that amplifier in which the operating point is such that the collector current flows for full cycle of the A.C signal.

Class 'B' Amplifiers :-

Class B amplifiers is that amplifier in which the operating point is such that the collector current flows for half cycle of input A.C signal.

Class 'C' Amplifiers :-

Class C amplifiers is that amplifier in which the operating point is such that the collector current flows for less than half cycle of A.C signal.

Question Bank

Fill in the blanks :-

1- The circuit that provides transistor biasing is known as _____.

2- _____ is the process of increasing the magnitude of a weak signal without any change in its shape.

3- _____ circuit provides transistor biasing.

4. _____ is changed if the temperature is changed or the transistor is replaced.

5. _____ is the process of making the operating point independent of temperature changes or variations in transistor parameters.

6. The collector leakage current I_{CBO} is affected by the _____ variation.

7. _____ is the self-destruction of an unstability transistor.

8. Stability factor of a biasing circuit is the rate of change of collector current with respect to _____ at constant β and I_B.

9. _____ is the ratio of output current to input current.

10. _____ is the ratio of output voltage to input voltage.

11. _____ is the ratio of output power to input power

12. voltage amplifier increases the _____ level of the signal.

13. Power amplifier increases the _____ level of the signal.

14. _____ are used to amplify the signals in the audio frequency range.

15. _____ are used to amplify the signals in the radio frequency range.

Short Note:- (2marks)

1. What are voltage amplifiers ?
2. What is power amplifiers ?
3. What are audio amplifiers ?
4. What is radio frequency amplifiers ?
5. What is RC-coupled amplifiers ?
6. What is transformer Coupled amplifiers ?
7. What are class A amplifiers ?
8. What is thermal runway ?
9. What are class-B amplifiers ?
10. What are class-C amplifiers ?
11. What are the stability factor ?
12. What is transistor biasing ?
13. What is stabilisation ?
14. What are the different method of biasing a transistor
15. What is voltage divider Bias ?

Short note for (3 marks)

1. What is transistor biasing ? What is the need for transistor biasing ?
2. What is stabilisation ? What is need of stabilisation
3. Describe the fixed bias method for transistor biasing. Write its advantages and disadvantages.
4. Describe the Collector-base bias method of transistor biasing write its advantage & dis
5. (a) Transistor as a two port network.
   (b) Stabilization of operating point.

Long question :-

① What is faithful amplification ? Discuss about the conditions for faithful amplification in a transistor amplifier.

② What are hybrid parameters ? Explain the hybrid equivalent circuit of a transistor.

③ Draw the hybrid equivalent circuit of a single stage CE amplifier. Find the expressions for input impedance, output impedance, current gain, voltage gain and power gain.

④ Draw the hybrid equivalent circuit of a single stage CC amplifier and find the expressions for input impedance, output impedance, current gain, voltage gain and power gain.

⑤ Discuss about the classification of amplifiers according to mode of operation.